SIS3610
VME Input/Output Register

User Manual

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Revision Table:

Revision	Date	Comment
0.10	27.07.02	Generation from SIS3601 manual
0.20	20.11.02	add JLAB/DUKE IRQ an Flipflop functionality
0.21	22.11.02	Add or of control inputs as latch condition
1.00	13.12.02	First official release
1.01	20.01.03	Bug fix in address map
1.02	05.03.03	IRQ setup sentence fix
1.10	02.11.04	Firmware Version 2 for 50 Ω TTL units
1.11	04.01.06	ESD note added
1.20	02.08.06	Bug fix in input/output numbering

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2 Introduction

The SIS3610 is a 16-bit input/16-bit output card on the base of the SIS36/38xx VME board family. It is a single width (4 TE) 6U (double euro form factor) card and combines part of the SIS3600 input register and SIS3601 output register functionality. The card was developed to act as a simple input/output module, which allows to set up to 16 output levels and to read up to 16 input levels in asynchronous slow control applications.

Applications for the card comprise, but are not limited to:

- read digital on/off status information (magnet, shutter, ...)
- read 1-bit to 16-bit wide pattern
- switch external hardware/flag status
- write 1-bit to 16-bit wide pattern
- interrupt generation
- deadtime FLIPFLOP

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm. A list of available firmware designs can be retrieved from http://www.struck.de/sis3638firm.htm

3 Technical Properties/Features

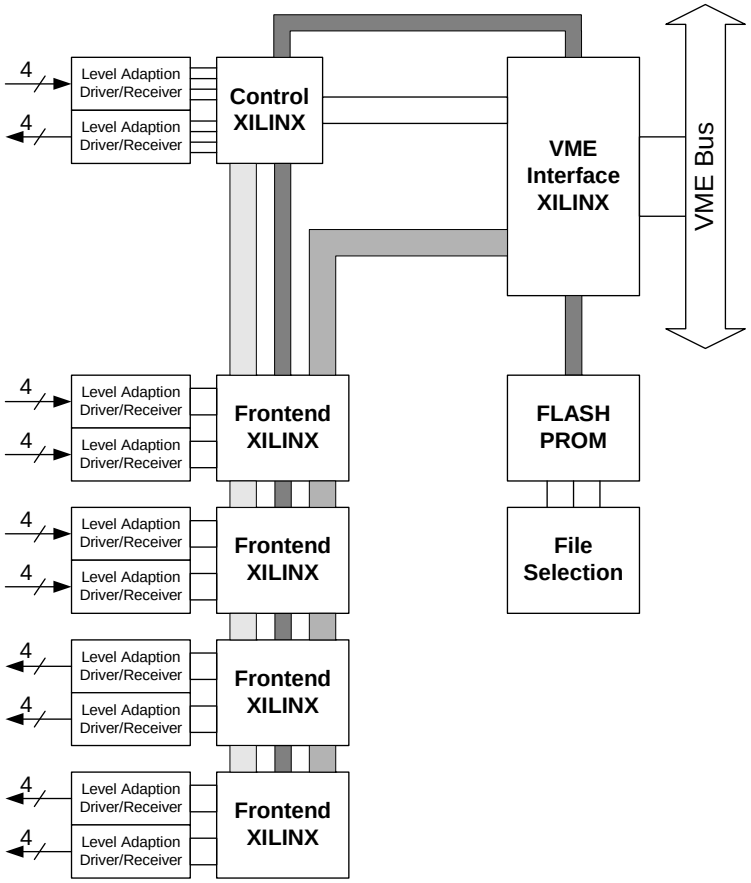
The SIS3610 is rather a firmware design in combination with given board stuffing options, than a name for the board (this is the reason, why the modules are named SIS36/38xx on the front panel and the distinction of the units is made by the module identifier register). The firmware makes use of part of the possibilities of the SIS36/38xx PCB, if the SIS3610 or other firmware designs of the family come close to what you need, but something is missing, a custom firmware design may be an option to consider.

Find below a list of key features of the SIS3610.

- 16-bit input
- 16-bit output
- 4 user outputs/flipflops (control section)
- interrupt generation
- common IRQ level up to 4 different IRQ vectors
- NIM/TTL/ECL/LVDS versions
- flat cable (TTL/ECL/LVDS) and LEMO (TTL/NIM) versions
- A16/A24/A32 D16/D32
- Base address settable via 5 rotary switches (A32-A12) and one jumper (A11)
- VIPA geographical addressing prepared
- VIPA LED set
- Up to eight firmware files
- single supply (+5 V)

3.1 Board Layout

Xilinx FPGAs are the working horses of the SIS36/38xx board series. The counter (prescaler, latch, ...) logic is implemented in one to four chips, each chip handles eight front end channels. The VME interface and the input and output control logic reside in two Xilinx chips also. The actual firmware is loaded into the FPGAs upon power up from a FLASHPROM under jumper control. The user can select among up to eight different boot files by the means of a 3-bit jumper array. The counter inputs, the control inputs and the outputs can be factory configured for ECL, LVDS, NIM and TTL levels. The front panel is available as flat cable (ECL, LVDS and TTL) or LEMO (NIM and TTL) version. The board layout is illustrated with the block diagram below:



SIS3610 Block Diagram

3.2 Design and Modus Operandi

The inputs and outputs are implemented in XILINX FPGAs. One of the FPGAs holds 8 channels (bits). The data are passed to and read from the frontend chips by the control FPGA. The outputs are set by writing to the direct output data or the J/K output register, readback of the data is supported also. The inputs are read from the input data register. In addition the 4 user outputs can be controlled via the control register, they are implemented in a J/K fashion, what allows the user to change a single bit without knowledge of the status of the other three bits.

4 Getting Started

The minimum setup to operate the SIS3610 requires the following steps:

- Check the proper firmware design is selected (should be design zero, i.e. all jumpers of jumper array J500 set.
- Select the VME base address for the desired addressing mode
- Select the VME SYSRESET behaviour via J520
- turn the VME crate power off
- install the in/output register in the VME crate
- connect your signals to the module
- turn crate power back on
- issue a key reset by writing to 0x60
- select latch strobe condition in control register
- set outputs by writing to direct output data or J/K output register
- read inputs by reading from the direct or latched input data register

A good way of checking first time communication with the SIS3610 consists of switching on the user LED by a write to the control register at offset address 0x0 with data word 0x1 (the LED can be switched back off by writing 0x100 to the control register)..

4.1 Factory Default Settings

4.1.1 Adressing

SIS3610 boards are shipped with the En_A32, the En_A24 and the En_A16 jumpers installed and the rotary switches set to:

Switch	SW_A32U	SW_A32L	SW_A24U	SW_A24L	SW_A16	J A_11	Bits 7-4	Bits 3-0
Setting	3	8	3	8	3	8	0	0

Jumper A_11 is open (bit 11 set).
Hence the unit will respond to the following base addresses:

Mode	Base address
A32	0x38383800
A24	0x383800
A16	0x3800

Firmware Design
Design 0 (SIS3610, Version 1) of the FLASHPROM is selected (all jumpers of jumper array J500 closed). Units with 50 Ω TTL levels are configured to boot design 1 (SIS3610, Version 2) for signal polarity reasons.

4.1.2 System Reset Behaviour

J520 is set, i.e. the SIS3610 is reset upon VME reset.

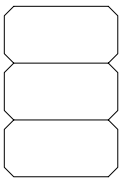
5 Firmware Selection

The FLASH PROM of a SIS36/38xx board can contain several boot files. A list of available FLASHPROM versions can be found on our web site http://www.struck.de in the manuals page. If your FLASHPROM has more than one firmware design, you can select the desired firmware via the firmware selection jumper array J500 . You have to make sure, that the input/output configuration and FIFO configuration of your board are in compliance with the requirements of the selected firmware design (a base board without FIFO can not be operated as multi channel scaler e.g.). A total of 8 boot files from the FLASHPROM can be selected via the three bits of the jumper array. The array is located towards the rear of the card between the VME P1 and P2 connectors. The lowest bit sits towards the bottom of the card, a closed jumper represents a zero, an open jumper a one.

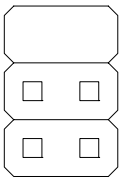
5.1 Examples

The figures below show jumper array 500 with the soldering side of the board facing the user and the VME connectors pointing to the right hand side.

Bootfile 0 selected
With all jumpers closed boot file 0 is selected



Bootfile 3 selected



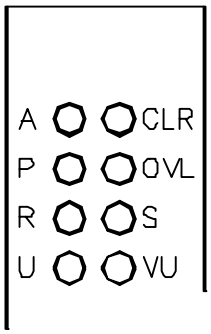
With the lowest two jumpers open bit 0 and bit 1 are set to 1 and hence boot file 3 is selected

Front Panel LEDs

The SIS3610 has 8 front panel LEDs to visualise part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 5 additional LEDs.

Designation	LED	Color	Function with SIS3610 design
A	Access	yellow	Signals VME access to the unit
P	Power	red	Flags presence of VME power
R	Ready	green	Signals configured logic
U	VME user LED	green	To be switched on/off under user program control
CLR	Out 4	yellow	Status of user output/Flipflop 4
OVL (CIP)	Out 3	red	Status of user output/Flipflop 3
S	Out 2	green	Status of user output/Flipflop 2
VU	Out 1	green	Status of user output/Flipflop 1

The LED locations are shown in the portion of the front panel drawing below.



The VME Access and the LNE LED are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status.
An LED test cycle is performed upon power up (refer to chapter 13.1).

6 VME addressing

6.1 Address Space

As bit 11 is the lowest settable bit on the 36/38xx board, an address space of 2 Kbytes (Offset plus 0x000 to 0x7ff) is occupied by the module.

6.2 Base Address

6.2.1 VME

The VME addressing mode (A16/A24/A32) is selected via the jumpers EN_A16, EN_A24 and EN_A32.The mode is selected by closing the corresponding jumper, it is possible to enable two or all three addressing modes simultaneously.
The base address is set via the five rotary switches SW_A32U, SW_A32L, SW_A24U, SW_A24L and SW_A16 and the jumper J_A11. The table below lists the switches and jumpers and their corresponding address bits.

Switch/Jumper	Affected Bits
SW_A32U	31-28
SW_A32L	27-24
SW_A24U	23-20
SW_A24L	19-16
SW_A16	15-12
J_A11	11

In the table below you can see, which jumpers and switches are used for address decoding in the three different addressing modes (fields marked with an x are used).

	SW_A32U	SW_A32L	SW_A24U	SW_A24L	SW_A16	J_A11
A32	x	x	x	x	x	x
A24			x	x	x	x
A16					x	x

Note: J_A11 closed represents a 0, J_A11 open a one

6.2.2 VIPA/VME64x

As the VME64x and the VME64xP (VIPA) standard were not yet standards to refer to and to declare conformity with at the point in time of the first SIS36/38xx firmware design developments, addressing modes (like geographical addressing e.g.) according to these standards are prepared but not yet implemented in the current firmware revisions.

6.3 Address Map

The SIS36/38xx boards are operated via VME registers, VME key addresses and the FIFO (where installed). The following table gives an overview on all SIS3610 addresses and their offset from the base address, a closer description of the registers and their function is given in the following subsections.

Offset	Key	Access	Type	Function
0x000		R/W	D16/D32	Control and status register
0x004		R/W	D16/D32	Module Identification register
0x008		R/W	D16/D32	direct output data register
0x00C		R	D16/D32	J/K output data register
0x010		R	D16/D32	direct input register
0x014		R	D16/D32	latched input register
0x060	KA	W	D16/D32	reset register (global reset)

Note: D08 is not supported by the SIS36/38xx boards

The shorthand KA stands for key address. Write access with arbitrary data to a key address initiates the specified function

7 Register Description

7.1 Status Register (0x0)

The status register reflects the current settings of theSIS3610 parameters, which have been set in write access to the control register (which resides at offset 0 also).

Bit	Function
31	Status VME IRQ source 3 (control input 4)
30	Status VME IRQ source 2 (control input 3)
29	Status VME IRQ source 1 (control input 2)
28	Status VME IRQ source 0 (control input 1)
27	VME IRQ
26	internal VME IRQ
25	0
24	0
23	Status VME IRQ Enable Bit source 3 (control input 4)
22	Status VME IRQ Enable Bit source 2 (control input 3)
21	Status VME IRQ Enable Bit source 1 (control input 2)
20	Status VME IRQ Enable Bit source 0 (control input 1)
19	Status Flipflop enable 4
18	Status Flipflop enable 3
17	Status Flipflop enable 2
16	Status Flipflop enable 1
15	0
14	0
13	0
12	0
11	0
10	0
9	0
8	0
7	Status user output 4
6	Status user output 3
5	Status user output 2
4	Status user output 1
3	Status latch strobe bit 1
2	Status latch strobe bit 0
1	Status interrupter style (0=RORA, 1=ROAK)
0	Status user LED

The reading of the status register after power up or key reset is 0x0 (see default settings of control register).

7.2 Control Register (0x0)

The control register allows the user to control the user LED and the user outputs of the SIS3610 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which has a different location within the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

Bit	Function
31	disable IRQ source 3 (control input 4) (*)
30	disable IRQ source 2 (control input 3) (*)
29	disable IRQ source 1 (control input 2) (*)
28	disable IRQ source 0 (control input 1) (*)
27	disable Flipflop 4 (*)
26	disable Flipflop 3 (*)
25	disable Flipflop 2 (*)
24	disable Flipflop 1 (*)
23	enable IRQ source 3 (control input 4) (*)
22	enable IRQ source 2 (control input 3) (*)
21	enable IRQ source 1 (control input 2) (*)
20	enable IRQ source 0 (control input 1) (*)
19	enable Flipflop 4
18	enable Flipflop 3
17	enable Flipflop 2
16	enable Flipflop 1
15	set user output 4 to 0 (*)/reset Flipflop 4
14	set user output 3 to 0 (*)/reset Flipflop 3
13	set user output 2 to 0 (*)/reset Flipflop 2
12	set user output 1 to 0 (*)/reset Flipflop 1
11	clear latch strobe bit 1
10	clear latch strobe bit 0
9	set RORA style interrupter/disable ROAK (*)
8	switch off user LED and clear user output (*)
7	set user output 4 to 1
6	set user output 3 to 1
5	set user output 2 to 1
4	set user output 1 to 1
3	set latch strobe bit 1 (0: leading edge of CTRL input 1, 1: change of input bit D0)
2	set latch strobe bit 0 (1: enable leading edge of OR of control inputs 1-4)
1	set ROAK style interrupter/disable RORA (*)
0	switch on user LED and set user output

(*) denotes the default power up or key reset state

7.2.1 Enable IRQ source/Interrupting

The four control inputs can be used for interrupt generation.
Following steps are required to set up the SIS3610 as interrupt generating VME slave:

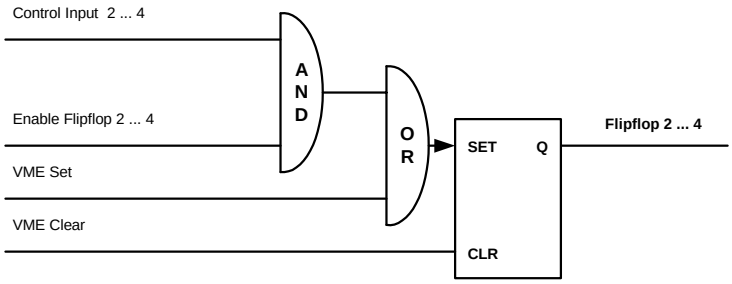
- select RORA/ROAK interrupter style in control register
- enable IRQ source (i.e. define which control inputs are active for input generation)
- define interrupt level and interrupt vector in the module id. and IRQ control register and set the VME IRQ enable bit in the same register

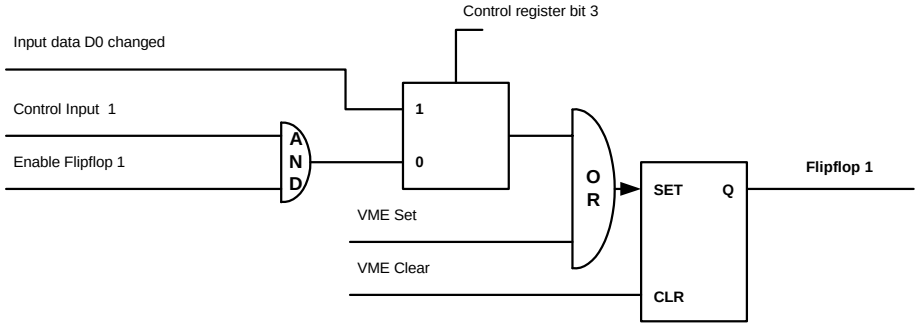
Note: The lowest four bits of the interrupt vector are defined by the status of the Flipflops and will allow for distinction between the control inputs if the OR condition is active.
This will allow you to implement different readout types for up to four different trigger types by taking the corresponding action in your interrupt service routine.

7.2.2 Flipflop enable

The control outputs of the SIS3610 can be operated as Flipflops. In Flipflop mode control output N is set with the leading edge of a signal on control input N and reset with the reset Flipflop N bit in the control register. Flipflop operation for output N is activated by setting the enable Flipflop N bit in the control register. The Flipflop logic is illustrated below.

Note: Flipflop 1 is set by a level change of input data bit 0 if bit 3 of the control register is set to 1 (latch strobe condition bit change). This feature can be used to one or several frontend crates by incrementing a up to 16-bit wide event number with the output section of another SIS3610 (or a SIS3610 in event number increment mode) in a "master crate".





7.3 Module Identification register (0x4)

This register has two basic functions. The first is to give information on the active firmware design. This function is implemented via the read only upper 20 bits of the register. Bits 16-31 hold the four digits of the SIS module number (like 3801 or 3610 e.g.), bits 12-15 hold the version number. The version number allows a distinction between different implementations of the same module number, the SIS3801 for example has the 24-bit mode with user bits and the straight 32-bit mode as versions. The second function is the definition of the VME IRQ level and vector and activation of VME interrupt generation.

Bit	Read/Write access	Function	
31	read only	Module Identification Bit 15	Module Id Digit 3
30	read only	Module Identification Bit 14	
29	read only	Module Identification Bit 13	
28	read only	Module Identification Bit 12	
27	read only	Module Identification Bit 11	Module Id Digit 2
26	read only	Module Identification Bit 10	
25	read only	Module Identification Bit 9	
24	read only	Module Identification Bit 8	
23	read only	Module Identification Bit 7	Module Id Digit 1
22	read only	Module Identification Bit 6	
21	read only	Module Identification Bit 5	
20	read only	Module Identification Bit 4	
19	read only	Module Identification Bit 3	Module Id Digit 0
18	read only	Module Identification Bit 2	
17	read only	Module Identification Bit 1	
16	read only	Module Identification Bit 0	
15	read only	Version Bit 3	
14	read only	Version Bit 2	
13	read only	Version Bit 1	
12	read only	Version Bit 0	
11	read/write	VME IRQ enable flag (0=IRQ disabled, 1=IRQ enabled)	
10	read/write	VME IRQ Level Bit 2	
9	read/write	VME IRQ Level Bit 1	
8	read/write	VME IRQ Level Bit 0	
7	read/write	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	
6	read/write	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	
5	read/write	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	
4	read/write	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	
3	read/write	IRQ Vector Bit 3; write with 0, read status FLIPFLOP 4	
2	read/write	IRQ Vector Bit 2; write with 0, read status FLIPFLOP 3	
1	read/write	IRQ Vector Bit 1; write with 0, read status FLIPFLOP 2	
0	read/write	IRQ Vector Bit 0; write with 0, read status FLIPFLOP 1	

Module identification and version example:

The register for a SIS3801 in straight 32-bit mode (version 1) reads 0x38011nnn, for a SIS3801 in 24-bit mode (version 2) it reads 0x38012nnn. (the status of the lower 3 nibbles is denoted with n in the example with all n's).

7.4 Output data registers 0x8 and 0xC

The output levels of the 16 outputs can be controlled by two registers

- direct output data register (read/write)
- J/K output register (write only)

The level will be set according to the last transaction to both registers and can be read back from the direct output data register (even if it was altered by the J/K output register). While it is most straightforward to define a complete pattern like an event number with the direct output data register, the J/K register can be used to set/clear or flip an individual bit only without the hassle to remember the previous state.

7.4.1 Direct output data register 0x8

This read/write register defines the data which are applied to the output drivers.

Bit	Function
31	unused read back as 0
...	...
16	unused read back as 0
15	Output Bit 15
14	Output Bit 14
13	Output Bit 13
12	Output Bit 12
11	Output Bit 11
10	Output Bit 10
9	Output Bit 9
8	Output Bit 8
7	Output Bit 7
6	Output Bit 6
5	Output Bit 5
4	Output Bit 4
3	Output Bit 3
2	Output Bit 2
1	Output Bit 1
0	Output Bit 0

The default state upon power up and key reset is 0x0, i.e. all outputs at 0

7.4.2 J/K output data register 0xC

The second way to control the output level of SIS3610 is access to this write only register. It is implemented in a J/K fashion. Writing a 1 to the set bit (bits 0-15) will set the corresponding bit will result in a logic 1 on the output. Writing a 1 to the clear bit (bits 16-31) will clear the output level. Priority is on set if both set and clear are 1 at the same time.
The current output pattern can be read back from the direct output register .

Bit	Function
31	Clear Output Bit 15
30	Clear Output Bit 14
29	Clear Output Bit 13
28	Clear Output Bit 12
27	Clear Output Bit 11
26	Clear Output Bit 10
25	Clear Output Bit 9
24	Clear Output Bit 8
23	Clear Output Bit 7
22	Clear Output Bit 6
21	Clear Output Bit 5
20	Clear Output Bit 4
19	Clear Output Bit 3
18	Clear Output Bit 2
17	Clear Output Bit 1
16	Clear Output Bit 0
15	Set Output Bit 15
14	Set Output Bit 14
13	Set Output Bit 13
12	Set Output Bit 12
11	Set Output Bit 11
10	Set Output Bit 10
9	Set Output Bit 9
8	Set Output Bit 8
7	Set Output Bit 7
6	Set Output Bit 6
5	Set Output Bit 5
4	Set Output Bit 4
3	Set Output Bit 3
2	Set Output Bit 2
1	Set Output Bit 1
0	Set Output Bit 0

7.5 Latched input data register 0x14

VME read access to this read only register returns previously latched data. The VME read cycle does not initiate a latch cycle (this functionality is covered by the direct input data register).

Bit	Function
31	unused read back as 0
...	...
16	unused read back as 0
15	Input Bit 15
14	Input Bit 14
13	Input Bit 13
12	Input Bit 12
11	Input Bit 11
10	Input Bit 10
9	Input Bit 9
8	Input Bit 8
7	Input Bit 7
6	Input Bit 6
5	Input Bit 5
4	Input Bit 4
3	Input Bit 3
2	Input Bit 2
1	Input Bit 1
0	Input Bit 0

7.5.1 Latch strobe conditions

The latch condition is defined qith bits 2 and 3 of the control register . as illustrated in the table below.

Bit 3	Bit 2	Condition
0	0	Leading edge of control input 1
0	1	Leading edge of OR of control inputs 1 to 4 not used
1	0	Status change of input bit 0
1	1	not used

It will depend on the nature of the application what strobe condition is adequate, examples are listed in the table below.

Condition	Application example
VME read access (read data from direct data register)	Asynchronous read of input status
Status change of input bit 0 (read data from latched data register)	Distribution of 16-bit event number across several crates.
Leading edge of control input (read data from latched data register)	Synchronous input status read upon external trigger
Leading edge of OR of control inputs (read data from latched data register)	Synchronous input status read upon different external triggers

7.6 Direct input data register 0x10

VME read access to this read only register latches the current input levels that are present on the 16 inputs and returns the latched input data.

Bit	Function
31	unused read back as 0
...	...
16	unused read back as 0
15	Input Bit 16
14	Input Bit 15
13	Input Bit 14
12	Input Bit 13
11	Input Bit 12
10	Input Bit 11
9	Input Bit 10
8	Input Bit 9
7	Input Bit 8
6	Input Bit 7
5	Input Bit 6
4	Input Bit 5
3	Input Bit 4
2	Input Bit 3
1	Input Bit 2
0	Input Bit 1

8 Input Configuration

SIS36/38xx boards are available for NIM, TTL and ECL input levels and in LEMO and flat cable versions. The boards are factory configured for the specified input level and connector type, input termination is installed.

9 Connector Specification

The four different types of front panel and VME connectors used on the SIS360x and SIS38xx boards are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
20 pin header	Control (flat cable versions)	DIN41651 20 Pin (AMP e.g.)
34 pin header	Inputs (flat cable versions)	DIN41651 34 Pin (AMP e.g.)
LEMO	Control and Input (LEMO versions)	LEMO ERN.00.250.CTL

10 Control Signals

10.1 Control Outputs

Four control output signals are defined in the SIS3610 firmware design.

Signal	Control Signal
User Output/Flipflop 4	8
User Output/Flipflop 3	7
User Output/Flipflop 2	6
User Output/Flipflop 1	5

10.2 Control Inputs

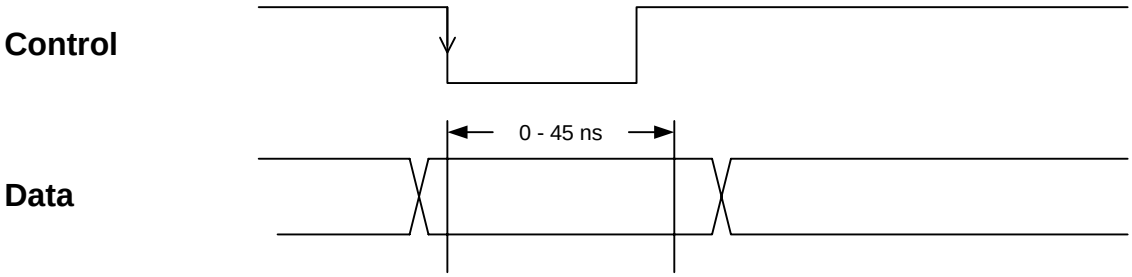
Four control input signals are defined in the SIS3610 firmware design. They can be used for interrupt generation and to set the Flipflop of the corresponding channel (to be reset by VME).

Signal	Control Signal
Control Input 4	4
Control Input 3	3
Control Input 2	2
Control Input 1	1

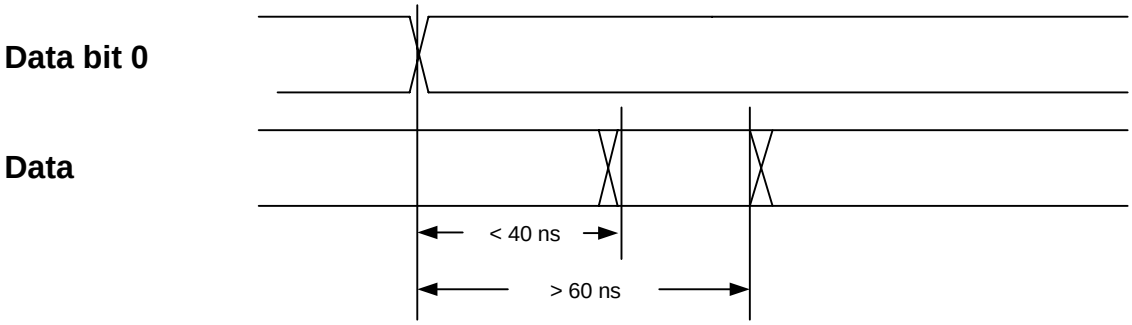
11 Signal timings

Signal timings are sketched in the diagrams below. Data have to be stable for > 45 ns after the strobe by the corresponding control signal or > 60 ns after the bit change induced strobe by data bit 0.

Strobe by control signal (NIM e.g.)



Strobe by data bit 0 change



12 Operating conditions

12.1 Power Consumption/Voltage requirement

Although the SIS3610 is prepared for a number of VIPA features, an on board DC/DC converter is used to generate the –5 V, which are needed for driver and receiver chips, to allow for the use of the module in all 6U VME environments. The power consumption is <17,5 W (+5V, <3,5A).

12.2 Cooling

Forced air flow is required for the operation of the SIS3610 board.

12.3 Insertion/Removal

Please note, that the VME standard does not support live insertion (hot swap). Hence crate power has to be turned off for installation and removal of SIS3610 output registers.
The leading pins on the SIS3610 VME64x VME connectors and connected on board circuitry are designed for hot swap in conjunction with a VME64x backplane (a VME64x backplane can be recognised by the 5 row VME connectors, while the standard VME backplane has three row connectors only).

13 Test

As the SIS3610 firmware is a rather simple design, it does not feature self test capabilities besides the power up self test of the module.

13.1 LED (selftest)

During power up self test and LCA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, all LEDs except the Ready (R) LED and the Power (P) have to go off. Differing behaviour indicates either a problem with the download of the firmware boot file or one or more LCA and/or the download logic.

14 Software Support

VME boards are tested at SIS with an OR VP6 VME CPU (Pentium II based) under Windows 95 and a National Instruments CVI user interface. The actual VME C code makes use of the OR Windows 95 DLL.
More recently testing of part of the modules is done with the SIS1100/3100 under LINUX or Windows2000/XP
In many cases the user setup will be using different hardware, a full fledged real time operating system like VxWorks, and a different user interface. We still believe, that it is helpful to have a look at the code which is used to test the units and to take it as an example for the implementation of the actual readout application. A CDROM with our SIS36/38xx test software (which is used to test the unit for the time being) is enclosed with SIS3610 shipments to first time users.

14.1 Contents of the included CDROM

Shipments to first time users are accompanied by the SIS36/38xx CDROM. The CDROM contains the PDF manuals for all modules of the family as well as test software for the modules for VP5/6/7 SBCs by SBS OR computers running under Windows 95. In addition C example code for the SIS1100/3100 PCI to VME interface for part of the modules is contained also.

15 Appendix

15.1 Address Modifier Overview

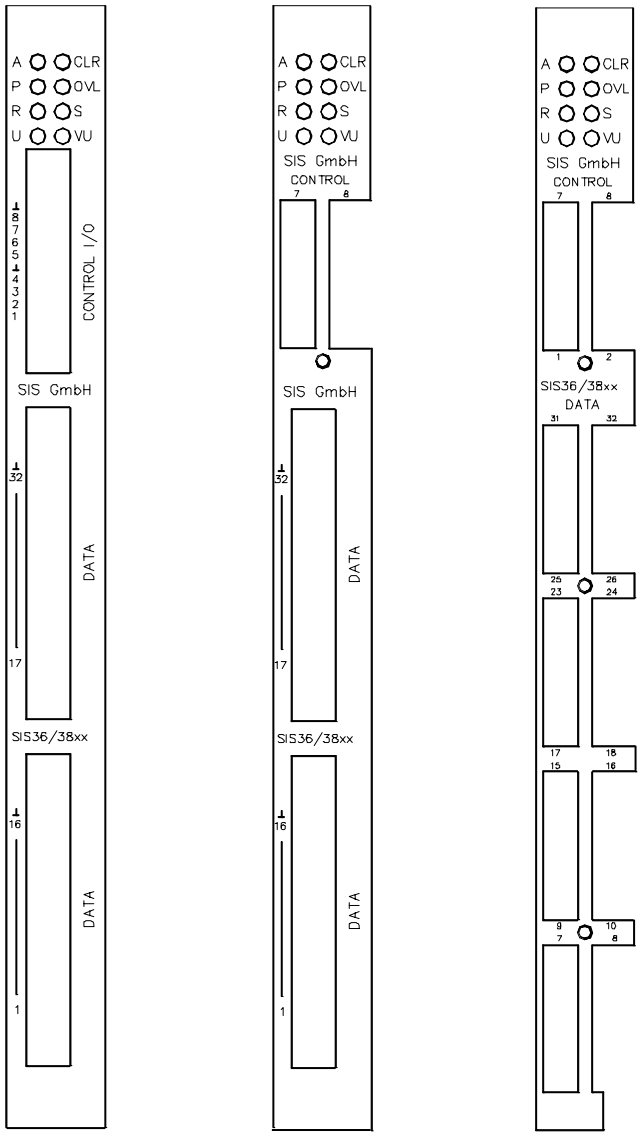
Find below the table of address modifiers, which can be used with the SIS36/38xx (with the corresponding addressing mode enabled).

AM code	Mode
0x3F	A24 supervisory block transfer (BLT)
0x3D	A24 supervisory data access
0x3B	A24 non-privileged block transfer (BLT)
0x39	A24 non-privileged data access
0x2D	A16 supervisory access
0x29	A16 non-privileged access
0x0F	A32 supervisory block transfer (BLT)
0x0D	A32 supervisory data access
0x0B	A32 non-privileged block transfer (BLT)
0x09	A32 non privileged data access
	Future option: CBLT

15.2 Front Panel Layout

The front panel of the SIS3610 is equipped with 8 LEDs, 8 control in- and outputs and 16 inputs and 16 outputs. On flat cable units (ECL, LVDS and TTL) the control connector is a 20 pin header flat cable connector and the channel inputs are fed via two 34-pin headers. On LEMO (NIM and TTL) units the control in- and outputs are grouped to one 8 channel block and the inputs/outputs are grouped into 2 blocks of 16 channels. The outputs are on data channels 1-16 (i.e. lower connector), the inputs on data channels 17-32 (i.e. upper connector). The units are 4 TE (one VME slot) wide, the front panel is of EMC shielding type. VME64x extractor handles are available on request or can be retrofitted by the user, if he wants to change to a VME64x crate at a later point in time.
In the drawing below you can find the flat cable (left hand side), the mixed (LEMO control, flat cable output, middle) and the LEMO (right) front panel layouts.

Note: Only the aluminium portion without the extractor handle mounting fixtures is shown



15.3 List of Jumpers

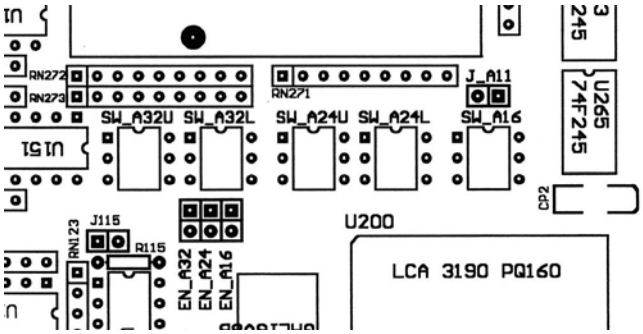
Find below a list of the jumpers and jumper arrays.

Jumper_Name	Array/Single	Function
J101	Single	Input Termination Control Input 1
J102	Single	Input Termination Control Input 2
J103	Single	Input Termination Control Input 3
J104	Single	Input Termination Control Input 4
J105	Single	Input Termination Control Input 5
J106	Single	Input Termination Control Input 6
J107	Single	Input Termination Control Input 7
J108	Single	Input Termination Control Input 8
J115	Single	Level Configuration (not for end user)
J500	Array	Boot File Selection
J520	Single	VME SYSRESET Behaviour
EN_A16	Single	Enable A16 addressing
EN_A24	Single	Enable A24 addressing
EN_A32	Single	Enable A32 addressing
J_A11	Single	Address Bit 11 Selection

15.4 Jumper and rotary switch locations

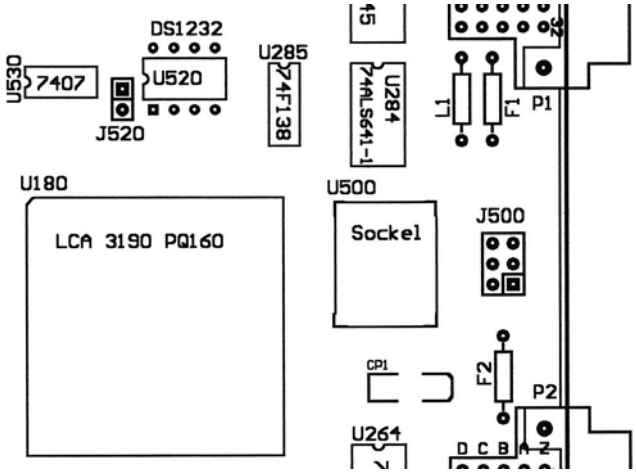
15.4.1 Addressing mode and base address selection

The EN_A32, EN_A24, EN_A16, A_11 and the 5 rotary switches are located int the middle of the upper section of the board close to the DC/DC converter, the corresponding section of the PCB is shown below.

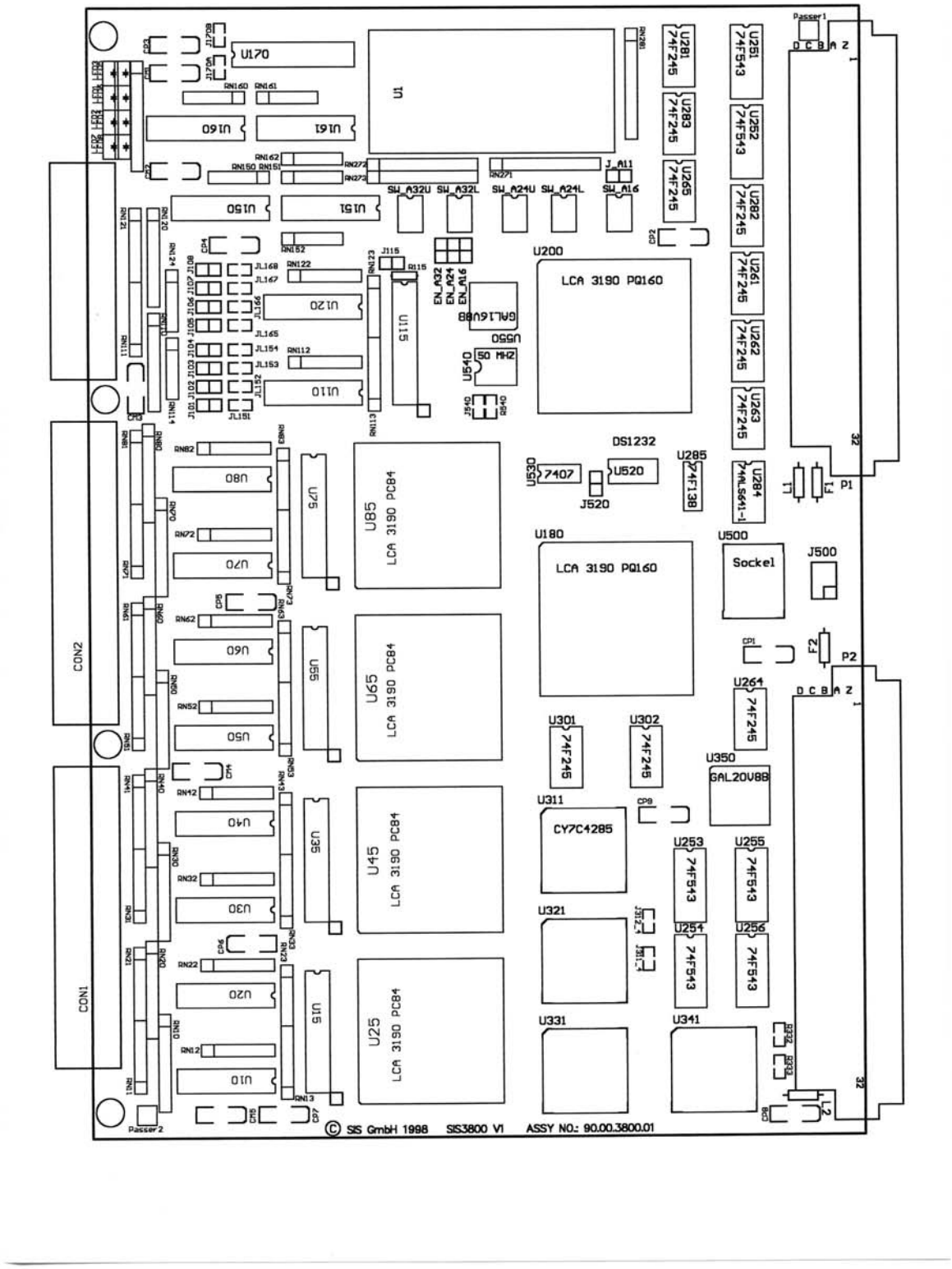


15.4.2 J500 (Bootfile Selection) and J520 (SYSRESET Behaviour)

The jumper array J500 is located between the P1 and the P2 connector. An open position in J500 defines a one (see also chapter 4), the lowest bit is next to the P2 connector.. J520 is located to the left of J500 and closer to the DC-DC converter. With jumper J520 closed the SIS3801 executes a key reset upon the VME SYSRESET signal. The section of the board with the jumper array and the SYSRESET jumper is shown below.

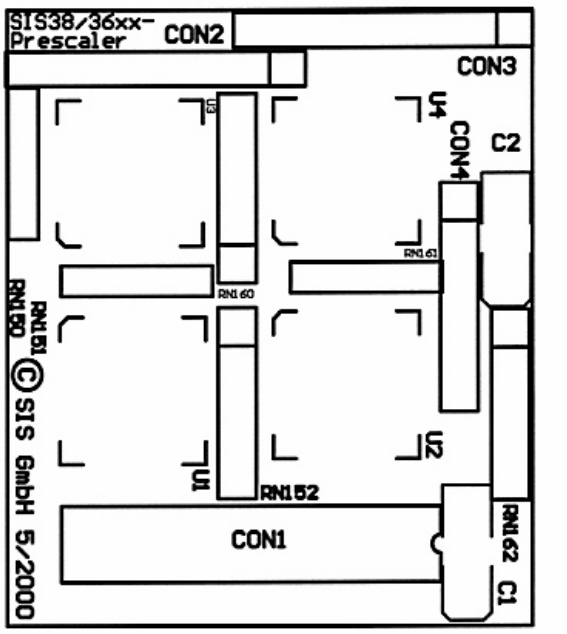


15.5 Board Layout



15.6 Driver Piggy Pack Layout

Driver piggy pack cards are installed on the two output groups of ECL and NIM level modules. Each of the cards drives 8 output bits. The top side of the driver card is shown below.



15.7 FLASHPROM Versions

A list of available FLASHPROMs can be obtained from http://www.struck.de/sis3638firm.htm. Please note, that a special hardware configuration may be necessary for the firmware design of interest (the SIS3801 design requires the installation of a FIFO e.g.).
The table on the web is of the format shown below:

SIS36/38xx FLASHPROM table

Design Name	Design	Boot File (s)
SIS3600_081298	0	SIS3600 Version 1
SIS3800_201098	0	SIS3800 Version 1
SIS3801_201098	0	SIS3800 Version 1
	1	SIS3800 Version 2
	2	SIS3801 Version 1 (32-bit Design)
	3	SIS3801 Version 2 (24-bit Design)
SIS3610_181004	0	SIS3610 Version 1
	1	SIS3610 Version 2

15.8 Row d and z Pin Assignments

The SIS3610 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

15.9 Geographical Address Pin Assignments

The SIS38xx board series is prepared for geographical addressing via the geographical address pins GA0*, GA1*, GA2*, GA3*, GA4* and GAP*. The address pins are left open or tied to ground by the backplane as listed in the following table:

Slot Number	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

15.10 Additional Information on VME

The VME bus has become a popular platform for many realtime applications over the last decade. Information on VME can be obtained in printed form, via the web or from newsgroups. Among the sources are the VMEbus handbook, http://www.vita.com (the home page of the VME international trade association (VITA)) and comp.bus.arch.vmebus. In addition you will find useful links on many high energy physics labs like CERN or FNAL

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